REMARKS

The Applicants request reconsideration of the rejection.

Claim 1-12, 14-17 and 19-43 are pending. Of these, Claims 1-7 and 21-43 have been withdrawn pursuant to a Restriction Requirement. Therefore, Claims 8-12, 14-17 and 19-20 have been examined on the merits.

Claims 8 and 14-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hiroyuki et al., JP 2000-188369 (corresponding to Juso, U.S. 6,181,002) in view of Takiar et al., U.S. 5,422,345 (Takiar). The Applicants traverse as follows.

In pertinent part, the invention claimed in Claim 8 is a semiconductor device manufacturing method including steps of preparing a wiring substrate having a plurality of electrodes created on a main surface thereof, preparing a first semiconductor chip having a plurality of protruding electrodes created on a main surface thereof, placing the first semiconductor chip on the main surface of the wiring substrate with the main surface of the first semiconductor chip facing the main surface of the wiring substrate so that the protruding electrodes on the first semiconductor chip face the electrode on the main surface of the wiring substrate,

electrically connecting all of the protruding electrodes simultaneously with corresponding electrodes of the wiring substrate while applying pressure to the back surface of the first semiconductor chip, preparing a second semiconductor chip having a plurality of electrodes created on a main surface thereof, placing the second semiconductor chip on the back surface of the first semiconductor chip so that the back surface of the second semiconductor chip faces the back surface of the first semiconductor chip, electrically connecting the electrodes on the second semiconductor chip on the main surface to corresponding electrodes on the wiring substrate by using a plurality of wires, and forming a resin sealing body for sealing the first and second semiconductor chips and the wires. Importantly, the second semiconductor chip has a thickness smaller than the thickness of the first semiconductor chip.

The Applicants direct the Examiner to Figure 1, which depicts a preferred example of the invention claimed in Claim 8. Note the wiring substrate 3, first semiconductor chip 1, and second semiconductor chip 2. The main surface 3a of the wiring substrate has electrodes 3c, and the main surface 1b of the first semiconductor chip 1 has protruding electrodes 1d facing the corresponding electrodes 3c (see also Figure 5(a)).

The second semiconductor substrate has electrodes 2a connected to electrodes 3c on the wiring substrate via wires 4.

In rejecting Claim 8, the Examiner asserts that Hiroyuki teaches a method including a step of preparing a wiring substrate 4 having a plurality of electrodes 6 created on a main surface thereof, and a step of placing a first semiconductor chip 1a on the main surface of the wiring substrate with the main surface of the first semiconductor chip facing the main surface of the wiring substrate so that protruding electrodes of the first semiconductor chip face the respected electrodes on the main surface on the wiring substrate. However, electrodes 6 of Hiroyuki's wiring substrate 4 are not prepared on the surface facing the semiconductor chip 1a. Therefore, the assertion in the Office Action does not appear to support the rejection.

Furthermore, due to an apparent typographical error (the column and line numbers asserted for the secondary reference to Takiar ("(10, 34-43)") have been inserted as referring to Hiroyuki's "protruding electrodes"), it is unclear what are considered to be protruding electrodes of Hiroyuki. Thus, the Applicants cannot ascertain the features alleged to correspond to the claimed protruding electrodes of the first semiconductor chip.

In this regard, there does not appear to be a clear teaching in Hiroyuki that the thicker semiconductor chip must be mounted to the wiring substrate via protruding electrodes by the claimed step of electrically connecting all of the protruding electrodes simultaneously with corresponding electrodes of the wiring substrate. The Applicants note that the step of applying pressure to the back surface of the first semiconductor chip during the "electrically connecting" step is alleged to be found in Takiar; however, fundamentally, Hiroyuki does not appear to teach the step alleged to be modified by Takiar to reach the invention.

Furthermore, the person of ordinary skill is not motivated to combine the asserted teachings of Takiar with those of Hiroyuki in order to achieve the present invention. As noted by the Examiner, Hiroyuki fails to teach the application of pressure to the first semiconductor chip so as to electrically connect protruding electrodes of the chip to the electrodes of the wiring substrate. Against this limitation, the Examiner cites Takiar at Column 10, lines 34-43, stating that the pressure bonding of Takiar is "conventionally known in the art" for bonding chips to substrates. However, Column 10, lines 34-43 of Takiar, in fact teach that an adhesive or soft-solder 48 is applied to

the principal mounting surface 40 of a carrier member 42, followed by dispensing a semiconductor die 22 onto the adhesive 48. Then, an adhesive or epoxy 50 is applied onto a first surface 30 of the die 22, and a first element 24 is then dispensed onto the adhesive 50. Nowhere is there a description of electrical connection of protruding electrodes of a semiconductor chip to electrodes of a wiring substrate by this pressure. Hiroyuki has no corresponding structure to that asserted in Takiar, and thus the person of ordinary skill could not know to modify Hiroyuki by the teachings of Takiar to reach the claimed invention.

Moreover, neither Hiroyuki nor Takiar recognize the importance of providing the thicker semiconductor chip as shown, so that the steps of electrically connecting the thicker semiconductor chip to the wiring substrate is performed by applying the pressure as claimed, and so that the relatively thinner semiconductor chip is adhered subsequently to the thicker semiconductor chip by applying pressure. The steps cannot be reversed (that is, the thinner semiconductor chip cannot be electrically connected to the wiring substrate by applying pressure to the second semiconductor chip, followed by adhering the thicker semiconductor chip to the back of the thinner semiconductor chip by applying pressure)

because the mounting load would cause chip crack problems which do not occur when the thicker semiconductor chip is the chip mounted by electrically connecting its protruding electrodes to the respective electrodes of the wiring substrate under pressure.

Claims 9 and 10 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hiroyuki in view of Takiar and Lau, "Flip Chip Technologies 1996" (Lau). Claims 11 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hiroyuki in view of Takiar and Okazaki et al., US 6,269,999 (Okazaki). Neither Lau nor Okazaki, however, provides the teachings missing from the attempted combination of Hiroyuki and Takiar discussed above.

Claims 17 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hiroyuki in view of Mitsuhiro, JP 3-106622 (Mitsuhiro) and Kumamoto et al., US 6,632,704 (Kumamoto). Claim 20 was rejected under 35 U.S.C. §103(a) as being unpatentable over Hiroyuki in view of Mitsuhiro and Kumamoto. Hiroyuki has been distinguished above. Mitsuhiro is cited as teaching a semiconductor molding process wherein a resin flows into a cavity containing a semiconductor package, wherein there exists two entrance gates on the same side of the cavity. Kumamoto is cited as teaching a molded flip-chip

package having air vents formed in the mold opposite the runner (resin injection entrance).

However, independent Claim 17 requires that, in placing the wiring substrate and semiconductor chips inside the cavity, the wiring substrate and semiconductor chips are arranged so that, on a cross section parallel to a third side surface of the cavity, the length of the first semiconductor chip exceeds the length of the second semiconductor chip; on a cross section parallel to the first side surface of the cavity, the length of the first semiconductor chip is smaller than the length of the second semiconductor chip; and that after placing the wiring substrate and semiconductor chips in the cavity in this way, resin is injected concurrently from the plurality of resin injection entrances toward the second side surface of the cavity in order to seal and hold the first and second semiconductor chips. By this feature of the invention, the resin flow is directed against a side having no overhang, which avoids the void formation in the flowing resin. In such a resin flow, the flowing resin runs up the stepped sides of the semiconductor chips and under the overhanging portions smoothly.

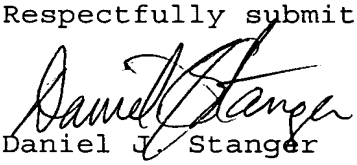
None of Hiroyuki, Mitsuhiro or Kumamoto teaches the advantage of directing resin flow in this way. Cherry-picking

individual features of the three references so as to reconstruct the claimed invention is the very definition of hindsight reasoning that is not permitted in making a prima facie case of obviousness. The Applicants note that the Examiner alleges motivation in the combination "because Kumamoto teaches that the air vents allow displaced air in the mold to escape" and "because Mitsuhiro teaches that heat can be absorbed effectively, pressure can be easily applied and the molding cycle time can be improved." However, none of the references directs the reader to inject the resin toward the second side surface of the cavity having the wiring substrate and semiconductor chips arranged as claimed. In particular, Hiroyuki does not teach a semiconductor device manufacturing method wherein the length of the first semiconductor chip exceeds the length of the second semiconductor chip viewed from one direction and is smaller than the length of the second semiconductor chip viewed from a different direction (that is, wherein respective cross sections taken parallel to the cavity side surfaces show an overhang in one direction and no overhang in the other direction), and Mitsuhiro does not suggest that the resin flow direction should be against an overhanging side or a non-overhanging side. Furthermore, none of the references suggests the advantage of providing the

resin flow in a desired direction with respect to overhanging or non-overhanging sides of the device to be sealed, let alone the advantage of preventing the generation of voids by performing all of the claimed steps in combination.

For each of the above reasons, the Applicants submit that the claimed invention patentably defines over the art of record, whether taken individually or in combination. Therefore, in view of the foregoing remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,



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